Abstract

A mixer circuit is configured using a CMOS transistor (800), comprising a p-channel transistor (840A) and an n-channel transistor (840B) in which semiconductor substrates (810A, 810) with at least two crystal planes and a gate insulator (820A) formed on at least two of the crystal planes on the semiconductor substrate are comprised and the channel width of a channel formed in the semiconductor substrate along with the gate insulator is represented by summation of each of the channel widths of channels individually formed on said at least two crystal planes. Such a configuration allows reduction of 1/f noise, DC offset generated in output signals due to variation in electrical characteristics of a transistor element, and signal distortion based on the channel length modulation effect.